Generating Hardware Assertion Checkers: For Hardware Verification, Emulation, Post-Fabrication Debugging and On-Line Monitoring

By Marc Boulé, Zeljko Zilic

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Assertion-based design is a powerful new paradigm that is facilitating quality improvement in electronic design. Assertions are statements used to describe properties of the design (I.e., design intent), that can be included to actively check correctness throughout the design cycle and even the lifecycle of the product. With the appearance of two new languages, PSL and SVA, assertions have already started to improve verification quality and productivity.

This is the first book that presents an "under-the-hood" view of generating assertion checkers, and as such provides a unique and consistent perspective on employing assertions in major areas, such as: specification, verification, debugging, on-line monitoring and design quality improvement.

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Editorial Review

From the Back Cover

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The PSL and SVA languages are treated in a unified way, thereby facilitating better learning and usage of the modern assertion languages, with a focus on obtaining the highest performance from assertion checkers.

The obtained checkers are thoroughly benchmarked and verified, while formal proofs using automated reasoning techniques are explained. Included are examples of practical circuits (PCI, AMBA, Wishbone-PIC, CPU Pipeline) and their assertion checker synthesis.

Users Review

From reader reviews:

David Jones:

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